APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/340,074	06/25/99	ARIMILLI R	AT9-98-781

	EXAMINER
	TZENG, F

ART UNIT	PAPER NUMBER
2186	

TM02/0605

ANDREW J DILLON
FELSMAN BRADLEY VADEN GUNTER & DILLONLLP
LAKEWOOD ON THE PARK SUITE 350
7600B NORTH CAPITAL OF TEXAS HIGHWAY
AUSTIN TX 78731

DATE MAILED:
06/05/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ___3___ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Mar 23, 2001* _____ .

2a) ☒ This action is **FINAL.** 2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-7, 10-18, and 21-27* _____ is/are pending in the application.

　　4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☐ Claim(s) _____ is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

　　a) ☐ All b) ☐ Some* c) ☐ None of:

　　　1. ☐ Certified copies of the priority documents have been received.

　　　2. ☐ Certified copies of the priority documents have been received in Application No. _____ .

　　　3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

　　*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☐ Notice of References Cited (PTO-892)　　　　　18) ☐ Interview Summary (PTO-413) Paper No(s). _____

16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)　　19) ☐ Notice of Informal Patent Application (PTO-152)

17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____　　20) ☐ Other: _____

DETAILED ACTION

1.   This office action is in responsive to the communication filed on March 23, 2001. Claims

1-7, 10-18 and 21-27 are now pending with claims 1, 10, 11 being amended and claims 22-27

being added newly.

2.   The objection to the specification is now withdrawn due the amendment filed on March

23, 2001.

Response to Arguments

3.   Applicant's arguments filed on March 23, 2001 have been fully considered but they are not

persuasive.

4.   In the remarks, applicants made one main point, i.e., "Patel clearly fails to discuss

selection of the victim cache block and certainly does not disclose selection of a victim in a lower

level cache utilizing cache hit information for an upper level cache.". This argument is not

persuasive as Patel clearly teaches when a request misses both L1 and L2 caches, the cache line is

sent to both L1 and L2, but is queued in the L2 reload queue for the transfer to L2 (i.e., a

selection of a victim in a L2 cache utilizing cache hit information of an L1 cache; see column 3

lines 5-10). This rationale makes the cited references related to applicants' claimed inventions.

Claim Rejections - 35 USC § 102

5.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6.   Claims 1-7, 10-18 and 21-27 are rejected under 35 U.S.C. 102(b) as being clearly

anticipated by Patel et al (USPN 5,737,751).

As to claim 1, Patel discloses a method of operating a multi-level cache of a computer

system (see column 2 lines 20-24), comprising the steps of: monitoring cache activity of an upper

level cache and a lower level cache both associated with a processor of the computer system (i.e.,

monitoring the cache activity of L1 cache 14 and L2 cache 20 which are both associated with the

processor 12 of the computer system 10; see figure 2 and column 5 lines 42-63); the monitoring

including monitoring cache hits in the upper level cache (see figure 3 and column 3 lines 5-10);

issuing a request from the processor to load a value, wherein the request misses the upper level

cache and the lower level cache (i.e., the processor 12 issues memory request to the multi-level

storage system which comprises L1 cache 14 and L2 cache 20, wherein the request misses both

the L1 cache 14 and L2 cache 20; see column 5 lines 42-44, 59-63); and selecting a victim cache

block in the lower level cache for receiving the requested value based at least in part on the prior

cache activity of the upper level cache (i.e., the reload queue of the L2 cache is selected for

receiving the requested value for sending to both L1 cache and L2 cache based on the prior cache

misses activity of L1 cache; see column 3 lines 5-10). By this rationale, claim 1 is rejected.

As to claim 2, Patel discloses that the victim cache block is further selected based in part

on the cache activity of the lower level cache (i.e., the reload queue of L2 cache is selected not

only based on the cache miss activity of L1 cache, but also based on the cache miss activity of the

lower level L2 cache; see column 3 lines 5-10). By this rationale, claim 2 is rejected.

As to claim 3, Patel discloses that the selecting step takes place out of a critical path of

execution of a core of the processor (i.e., the selecting steps are taking place from the execution

unit of processor 12; see column 4 lines 40-50). By this rationale, claim 3 is rejected.

As to claim 4, Patel discloses that the issuing step issues a request to load operand data

(i.e., the CPU requests a block of data or instructions from cache; see column 1 lines 66-67). By

this rationale, claim 4 is rejected.

As to claim 5, Patel discloses that the selecting step includes the step of identifying a less

recently used cache block in the lower level cache (see column 3 lines 27-30).

As to claim 6, Patel discloses the steps of: returning the requested value to the processor,

determining that it would be efficient to currently load into the upper level cache a cache line

which includes the requested value and in response to the determining step, loading the cache line

into the upper level cache (i.e., when the processor issues a store request for data, the requested

data is loaded only to the upper level L1 cache and the processor; see column 4 lines 4-7). By

this rationale, claim 6 is rejected.

As to claim 7, Patel discloses that the monitoring step monitors cache misses of the upper

level and lower level cache and the selecting step selects the victim cache block based at least in

part on the cache misses of the lower level cache (see column 5 lines 59-63). By this rationale,

claim 7 is rejected.

As to claim 10, Patel discloses the steps of selecting a victim cache block in the upper

level cache for receiving the requested value based at least in part on the cache activity of the

lower level cache (i.e., when the processor issues a store request after detecting the memory

request misses of both L1 cache and L2 cache, the retrieved cache lines are stored in the upper

level L1 cache only; see column 4 lines 4-7). By this rationale, claim 10 is rejected.

As to claims 11 and 22, Patel discloses a computer system (i.e., the computer system 10

depicted in figure 2; see column 4 lines 37-38), comprising: a system memory device (i.e., the

main memory 22 in figure 2; see column 5 lines 8-11); means for processing program instructions

(i.e., the processor 12; see column 4 lines 40-50); means connected to the processing means for

caching values stored in the system memory device, the caching means having at least an upper

level cache and a lower level cache both associated with the processing means (i.e., the upper

level L1 cache 14 and lower level L2 cache; see figure 2 and column 4 lines 51-67); means for

monitoring cache activity of the upper level cache and lower level cache (see column 5 lines 59-

63) including cache hits in the upper level cache (see column 3 lines 5-10); and means for

selecting a victim cache block in the lower level cache for receiving a value specified in a load

request issued by the processing means, wherein the load request missed the upper level cache and

the lower level cache, based at least in part on the cache activity of the upper level cache (see

column 3 lines 5-10). By this rationale, claims 11 and 22 are rejected.

As to claim 12, Patel discloses that the selecting means is located out of a critical path of

execution of a core of the processing means (i.e., the execution unit of processor 12; see column 4

lines 40-50). By this rationale, claim 12 is rejected.

As to claims 13 and 23, Patel discloses that the upper level cache is an operand data cache

(i.e., the L1 Icache and L1 Dcache; see column 2 lines 34-35). By this rationale, claims 13 and 23

are rejected.

As to claim 14, Patel discloses that the selecting means identifies a less recently used cache

block in the upper level cache (see column 3 lines 27-34). By this rationale, claim 14 is rejected.

As to claim 15, Patel discloses that the upper level cache is an L1 cache and the lower

level cache is an L2 cache (see figure 2 and column 4 lines 51-67). By this rationale, claim 15 is

rejected.

As to claims 16 and 24, Patel discloses that the upper level cache is a store-through cache

(i.e., any data stored in the upper level L1 cache is also stored in the L2 cache; see column 2 lines

36-45). By this rationale, claims 16 and 24 are rejected.

As to claims 17 and 25, Patel discloses the means for returning the requested value to the

processing means in response to the load request missing the upper level cache and the means for

loading a cache line which includes the requested value into the upper level cache in response to a

determination that it would be efficient to currently load the cache line into the upper level cache

(i.e., when the processor issues a store request for data, the requested data is loaded only to the

upper level L1 cache and the processor; see column 4 lines 4-7). By this rationale, claims 17 and

25 are rejected.

As to claims 18 and 26, Patel discloses that the monitoring means monitors cache misses

of the lower level cache and the selecting means selects the victim cache block based at least in

part on the cache misses of the lower level cache (see column 5 lines 59-63). By this rationale,

claims 18 and 26 are rejected.

As to claims 21 and 27, Patel discloses the means for selecting a victim cache block in the

upper level cache for receiving the requested value based at least in part on the cache activity of

the lower level cache (i.e., when the processor issues a store request after detecting the memory

request misses of both L1 cache and L2 cache, the retrieved cache lines are stored in the upper

level L1 cache only; see column 4 lines 4-7). By this rationale, claims 21 and 27 are rejected.

Conclusion

7.   The prior art made of record and not relied upon is considered pertinent to applicant's

disclosure.

8.   **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time

policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date

of this final action.

9.   **Any response to this office action should be mailed to:**

      Commissioner of Patents and Trademarks

      Washington, D.C. 20231

  or faxed to:

      (703) 308-9051, (formal communications, please mark

"EXPEDITED PROCEDURE")

  Or:

      (703) 308-6606 (for informal or draft communications, please label

      "PROPOSED" or "DRAFT")

      Hand-delivered responses should be brought to Crystal Park II, 2021

Crystal Drive, Arlington. V.A., Sixth Floor (receptionist).

10.   Any inquiry concerning this communication or earlier communications from the examiner

should be directed to Fred F. Tzeng whose telephone number is (703) 305-4841. The examiner

can normally be reached on weekdays from 9:30 am to 6:00 pm. The examiner can also be reached on alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim, can be reached on (703) 305-3821. The fax phone number for the organization where this application or proceeding is assigned is (703) 305-9731.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Fred F. Tzeng

June 03, 2001

MATTHEW KIM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100